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| First Named Inventor | : Heinrich-Martin BOEHM | | |
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Title : Method and Circuit for Conforming an Analog Actual
Signal to a Digital Desired Signal

## SUBMISSION OF SUBSTITUTE SPECIFICATION

Mail Stop Amendment
Commissioner for Patents                                            February 18, 2005
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Examiner's requirement in the Office Action dated November

18, 2004, please accept the attached Substitute Specification and a marked-up copy of

the original specification.   I certify that said substitute specification contains no new

matter and includes the changes indicated in the marked-up copy of the original

specification.

Respectfully submitted,

*Gary R Edwards*

Gary R. Edwards
Registration No. 31,824

CROWELL & MORING LLP
Intellectual Property Group
P.O. Box 14300
Washington, DC 20044-4300
Telephone No.: (202) 624-2500
Facsimile No.: (202) 628-8844
GRE:kms
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# METHOD AND CIRCUIT FOR  CONFORMING AN ANALOG ACTUAL SIGNAL TO A DIGITAL DESIRED SIGNAL

## BACKGROUND AND SUMMARY OF THE INVENTION

**[0001]**     This application claims the priority of ~~German patent document~~ German patent document 103 03 347.5, filed January 29, 2003, the disclosure of which is expressly incorporated by reference herein.

**[0002]**     The invention relates to a method and to a circuit for ~~conforming~~ changing an analog actual signal to a digital desired signal.

**[0003]**     RF systems are known which have RF (radio frequency) amplifiers as detectors (e.g., rf detectors or current sensors) for monitoring the transmitting and receiving operation.  In this case, a detected video signal is an image of received rf pulses, which are monitored by analog comparators and compared with a reference threshold.  The output of these comparators is analyzed, and the result is normally forwarded by way of serial interfaces for further processing.

**[0004]**     Referring to Figure 1, the [[The]] (normally programmable) analog ~~comparators~~ ~~K generate~~ comparator K generates the reference threshold (the analog desired signal $AS_S$) internally by means of an installed digital-to-analog converter D/A.  The corresponding digital values $DS_S$ for the analog desired signal $AS_S$ are stored in a known

storage medium SP, such as an EPROM and, depending on the operating mode of the comparator K, are written into the corresponding comparator input 1. The analog actual signal $S_I$ is fed to the other comparator input 2. At the comparator output A, it can be determined whether the actual signal [[$I_S$ ]] $\underline{S_I}$ is larger or smaller than the desired signal $AS_S$ (Figure 1).

[0005]   For calibrating the detectors, the rf power to be monitored is measured, for example, by means of an RF power meter (the so-called Peak Power Analyzer). Simultaneous, for the same rf pulse, the detected voltage must be measured at the detector, normally by means of an oscilloscope, at the output pin of the respective comparator.

[0006]   The high construction cost and time expenditures required for the measuring operation at the comparator output as described above are disadvantageous. Normally, no test pins or external plug connections are available at the output of the comparator, because this requires considerable additional expenditures during the production. Thus, for testing purposes, the entire apparatus must be reconstructed (for example, opened) in order to detect the actual signal at the comparator input. This creates measuring uncertainties because of tolerances at the measuring point in time by means of the oscilloscope, and measuring faults as a result of, for example, coupled-in interferences which falsify the actual signal. These measuring uncertainties therefore lead to disadvantages during the calibration of the detectors.

[0007]    Other disadvantages result from the fact that certain detectors may have to be calibrated at different temperatures and thus in climatic test chambers, making the adaptation of the test signals more difficult.

[0008]    It is an object of the invention to provide a simple, rapid, substantially automatic method for ~~adjusting~~ changing an analog actual signal to a digital desired signal.

[0009]    Another object of the invention is to provide such a method, by which an adaptive calibration of detectors becomes possible.

[0010]    Still another object of the invention is to provide a circuit for implementing the method.

[0011]    These and other objects and advantages are achieved by the method and apparatus according to the invention, in which the digital input signal fed to the digital/analog converter is adapted as a function of the output signal of the comparator present at the comparator output in a definable number of iterative steps (between definable lower and upper thresholds) according to a balancing method. The digital input signal fed to the digital/analog converter corresponds to the digital desired signal to which the analog actual signal is conformed.

[0012]    Other objects, advantages and novel features of the present invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0013]**    Figure 1 shows a known circuit for ~~conforming~~ converting an analog actual signal to a digital desired signal; [[and]]

**[0014]**    Figure 2 shows an embodiment of a circuit for implementing the method according to the invention; and [[.]]

**[0014.1]**    Figure 3 is a schematic depiction of input pulse burst which make up the analog actual signal.

## DETAILED DESCRIPTION OF THE DRAWINGS

**[0015]**    In the method according to the invention, [[the]] a reference threshold is prepared in a binary manner, as a function of the number of definable iterative steps, which advantageously corresponds to the bit length by which the digital desired signal is to be indicated. With a large number of iterative steps, the precision of the desired signal and of the reference threshold can therefore be indicated. Thus, in the case of eight iterative steps, the analog actual signal is simulated by ~~means of~~ an eight-bit resolution. In this case, the simulation takes place bit by bit according to the well known balancing method, in which the voltage present at the comparator is successively approximated in several steps. In digital technology, such a method is known for the implementation of A/D and/or D/A converters, in addition to the parallel method and the counting method.

**[0016]**    The method according to the invention eliminates the need for the test by means of an oscilloscope and its external adaptation. Additional time-intensive and cost-

intensive reconstructing measures are also eliminated, and the calibration can be carried out simply and rapidly without reconstruction in a climatic test chamber.

[0017]     In an ~~advantages~~ <u>advantageous</u> embodiment of the invention, the analog actual signal comprises a burst (pulse train) with several pulses having a definable pulse duration. The pulse duration may, for example, be in the range of only a few μsec. A burst may comprise any arbitrary number of pulses (for example 268)<u>, as shown schematically in Figure 3 of the drawing</u>.

[0018]     As a result of the successive pulses, for example, in the case of RF power transistors, a change of the actual signal may take place during the burst (a so-called burst droop) due to heating. During measurements, it was surprisingly found that, during the regular sending of bursts, the same conditions (constant actual value) always occur for the same pulses in the burst. In a further advantageous embodiment of the invention, the actual signal at the comparator is considered for a ~~definable reference~~ <u>preselectable</u> pulse <u>m</u> from the burst. Furthermore, on the basis of ~~this reference~~ <u>the preselected</u> pulse <u>m</u>, the signal value corresponding to the pulse center is advantageously processed in the comparator. <u>(See Figure 3.)</u>

[0019]     Thus, during the continuous operation of, for example, burst n to burst n+8 at pulse m, the analog actual value is ~~simulated~~ <u>converted</u> into a digital ~~desired~~ value.

[0020]     As a result of electromagnetic compatibility interferences (for example, so-called spikes), the generated digital desired signal may be falsified. In an advantageous

embodiment of the invention, in two additional iterative steps burst n+9 and burst n+10) the digital desired signal is verified. In this case, in a first step, a definable signal value (for example, 10% of the typical maximum value) is subtracted from the obtained digital desired signal (only if the digital desired signal previously had a correspondingly high value). When the present actual signal (at the ~~reference~~ <u>preselected</u> pulse) is compared with the desired signal (reduced by the difference) the former must exceed the latter. If not, the obtained desired value for this cycle is rejected. The corresponding result is recorded in a status bit. In the last step (burst n+10), a definable signal value (for example, 10% of the typical maximum value) is added beforehand to the desired signal, if the value is lower than the maximum value. When comparing the present actual signal (at the reference pulse) with the desired signal (reduced by the difference), a falling-short has to occur. If not, the obtained desired value for this cycle is rejected. The corresponding result is recorded in a status bit.

[0021]    The thus obtained desired values including the evaluation by status bits are transmitted by way of an existing bus system from the test object to an external testing computer. Depending on the requirements and data which originate from other sources (for example, a Peak Power Meter), the testing computer computes individual desired values as operating thresholds. The values of those operating thresholds are finally programmed in the EPROMS of the test object.

**[0022]** During the operation, the respective comparator monitors the detected pulse power with respect to a reference value which was previously loaded from the corresponding EPROM into the input register of the DA converter in the comparator.

**[0023]** Figure 2 shows an example of a circuit for implementing the method according to the invention. The circuit comprises a comparator K with two input ports 1, 2 and one output port A as well as a digital-to-analog converter D/A with one digital input port $D_E$ and one analog output port $D_A$. The analog output port $D_A$ is connected with an input port 1 of the comparator K. The analog actual signal $I_S$ to be adapted is fed to the other input port 2 of the comparator K. The output port A of the comparator K is connected with an electronic component KV for generating a digital desired signal $DS_S$, which is fed to the digital input port $D_E$ of the digital-to-analog converter D/A. In this case, the electronic component KV is constructed such that it generates the digital desired signal $DS_S$ according to the balancing method.

**[0024]** The digital desired signal $DS_S$ generated by the electronic component KV can also be fed to additional components (not shown) for a further processing.

**[0025]** The circuit illustrated in Figure 2 permits, for example, the generation of a threshold value for a certain operating mode in the calibrating mode for an RF detector of an RF apparatus.

**[0026]** The foregoing disclosure has been set forth merely to illustrate the invention and is not intended to be limiting. Since modifications of the disclosed embodiments

incorporating the spirit and substance of the invention may occur to persons skilled in the art, the invention should be construed to include everything within the scope of the appended claims and equivalents thereof.

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